



Dual N-Channel 60-V (D-S) MOSFET

| PRODUCT SUMMARY | | | |
|-----------------|---------------------------|-----------|-------------|
| V_{DS} (V) | $r_{DS(on)}$ (Ω) | I_D (A) | Q_g (Typ) |
| 60 | 0.060 @ $V_{GS} = 10$ V | 4.8 | 13 |
| | 0.075 @ $V_{GS} = 4.5$ V | 4.3 | |

FEATURES

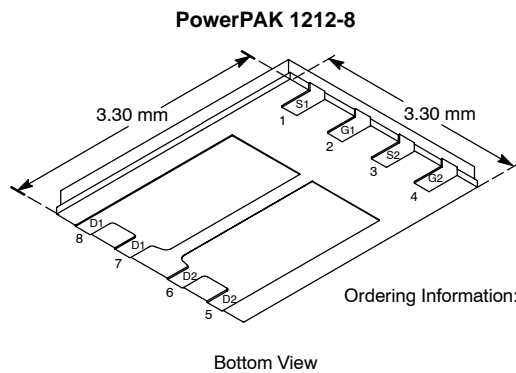
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package, 1/3 the Space of An SO-8 While Thermally Comparable



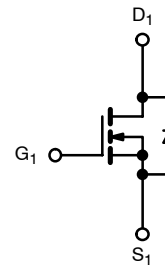
RoHS
COMPLIANT

APPLICATIONS

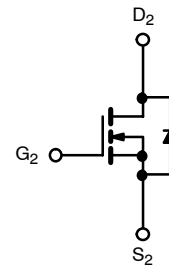
- Synchronous Rectification
- Primary Side Switch



Ordering Information: Si7220DN-T1—E3 (Lead (Pb)-Free)



N-Channel MOSFET



N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED) | | | | | |
|---|----------------|--------------------------|--------------|------------------|---|
| Parameter | Symbol | 10 secs | Steady State | Unit | |
| Drain-Source Voltage | V_{DS} | 60 | | V | |
| Gate-Source Voltage | V_{GS} | ± 20 | | | |
| Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a | I_D | $T_A = 25^\circ\text{C}$ | 4.8 | 3.4 | A |
| | | $T_A = 70^\circ\text{C}$ | 3.8 | 2.7 | |
| Pulsed Drain Current | I_{DM} | 20 | | | |
| Avalanche Current | $L = 0.1$ mH | I_{AS} | 11 | | |
| Single Avalanche Energy | | | E_{AS} | 6.1 | |
| Continuous Source Current (Diode Conduction) ^a | I_S | 2.2 | 1.1 | A | |
| Maximum Power Dissipation ^a | P_D | $T_A = 25^\circ\text{C}$ | 2.6 | 1.3 | W |
| | | $T_A = 70^\circ\text{C}$ | 1.4 | 0.69 | |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | -55 to 150 | | $^\circ\text{C}$ | |
| Soldering Recommendations (Peak Temperature) ^{b,c} | | 260 | | | |

| THERMAL RESISTANCE RATINGS | | | | | |
|--|------------|-----------------|---------|------|---------------------------|
| Parameter | Symbol | Typical | Maximum | Unit | |
| Maximum Junction-to-Ambient ^a | R_{thJA} | $t \leq 10$ sec | 38 | 48 | $^\circ\text{C}/\text{W}$ |
| | | Steady State | 77 | 94 | |
| Maximum Junction-to-Case (Drain) | R_{thJC} | 4.3 | 5.4 | | |

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- See Solder Profile (<http://www.vishay.com/doc?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.



Si7220DN

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SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

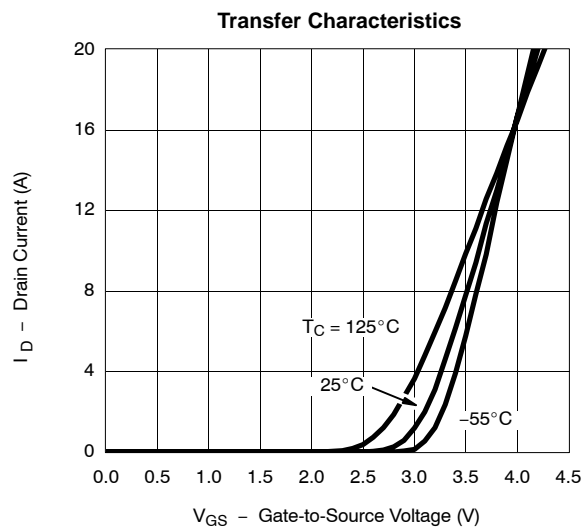
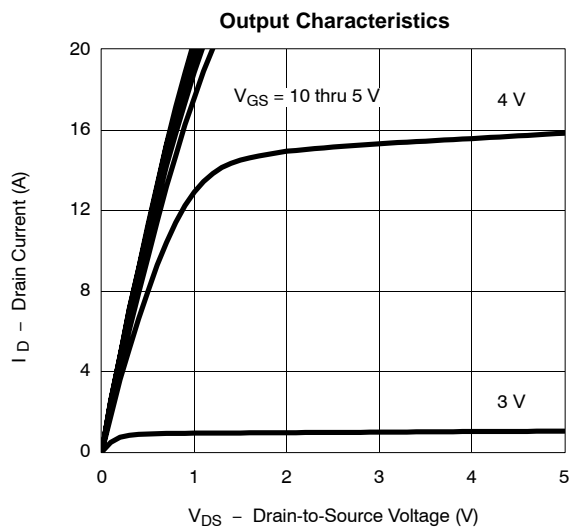
| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------|--|-----|-------|-------|------|
| Static | | | | | | |
| Gate Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | 1 | | 3 | V |
| Gate-Body Leakage | I _{GSS} | V _{DS} = 0 V, V _{GS} = ±20 V | | | ±100 | nA |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 60 V, V _{GS} = 0 V | | | 1 | μA |
| | | V _{DS} = 60 V, V _{GS} = 0 V, T _J = 85 °C | | | 5 | |
| On-State Drain Current ^a | I _{D(on)} | V _{DS} ≥ 5 V, V _{GS} = 10 V | 20 | | | A |
| Drain-Source On-State Resistance ^a | r _{DS(on)} | V _{GS} = 10 V, I _D = 4.8 A | | 0.048 | 0.060 | Ω |
| | | V _{GS} = 4.5 V, I _D = 4.3 A | | 0.061 | 0.075 | |
| Forward Transconductance ^a | g _{fs} | V _{DS} = 10 V, I _D = 4.8 A | | 15 | | S |
| Diode Forward Voltage ^a | V _{SD} | I _S = 2.2 A, V _{GS} = 0 V | | 0.8 | 1.2 | V |
| Dynamic^b | | | | | | |
| Total Gate Charge | Q _g | V _{DS} = 30 V, V _{GS} = 10 V, I _D = 4.8 A | | 13 | 20 | nC |
| Gate-Source Charge | Q _{gs} | | | 2.3 | | |
| Gate-Drain Charge | Q _{gd} | | | 2.6 | | |
| Gate Resistance | R _g | f = 1 MHz | | 2 | | Ω |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = 30 V, R _L = 30 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 6 Ω | | 10 | 15 | ns |
| Rise Time | t _r | | | 10 | 15 | |
| Turn-Off Delay Time | t _{d(off)} | | | 20 | 30 | |
| Fall Time | t _f | | | 10 | 15 | |
| Source-Drain Reverse Recovery Time | t _{rr} | I _F = 2.2 A, di/dt = 100 A/μs | | 30 | 60 | |

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

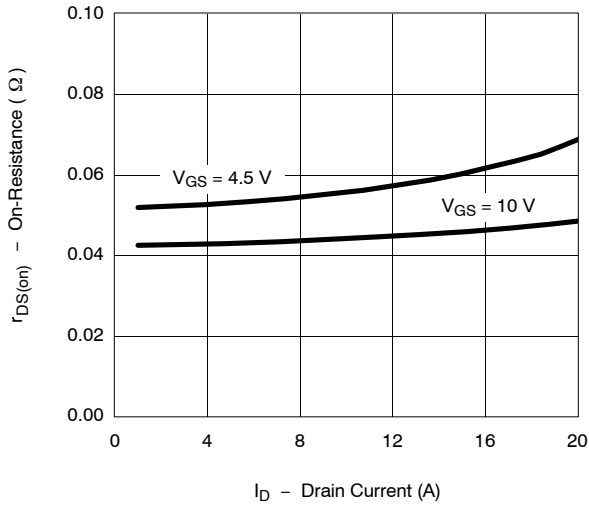
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



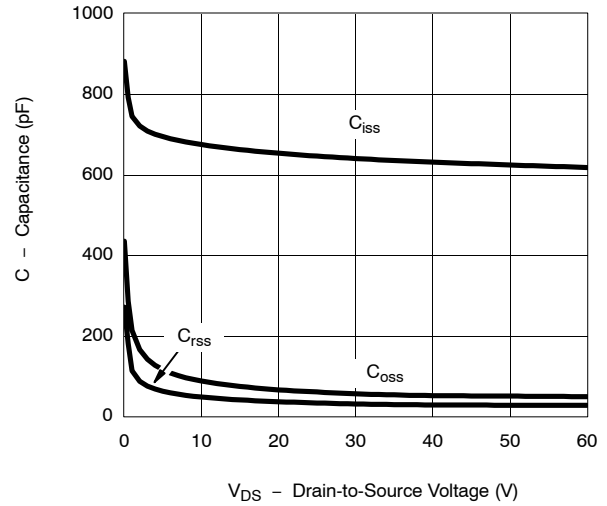


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

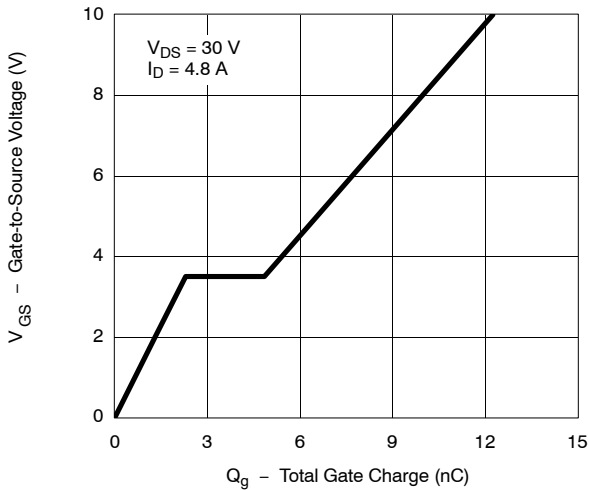
On-Resistance vs. Drain Current



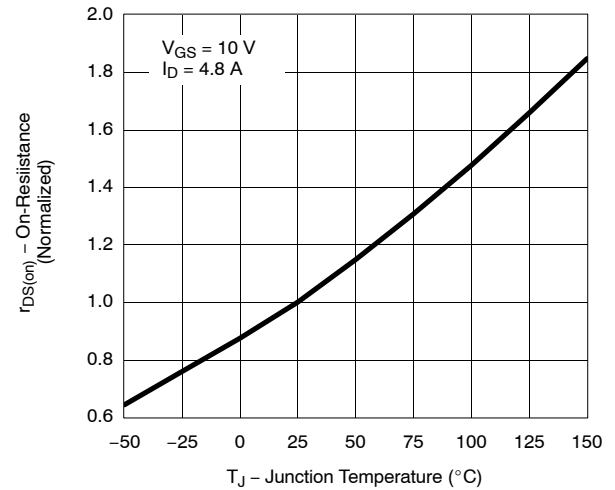
Capacitance



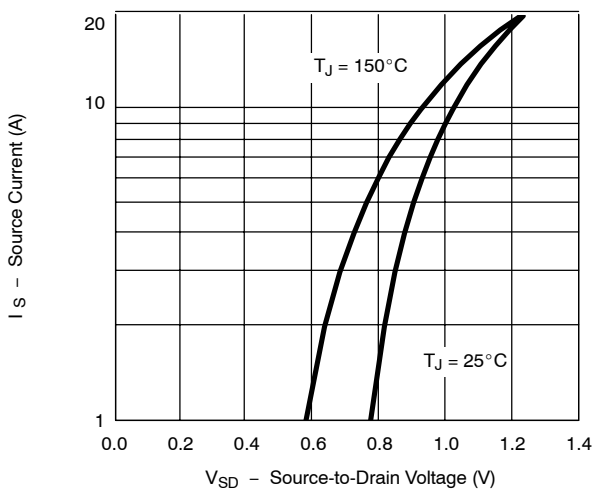
Gate Charge



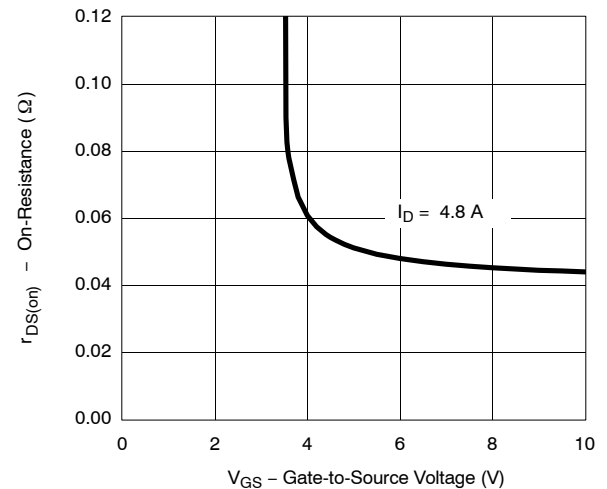
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

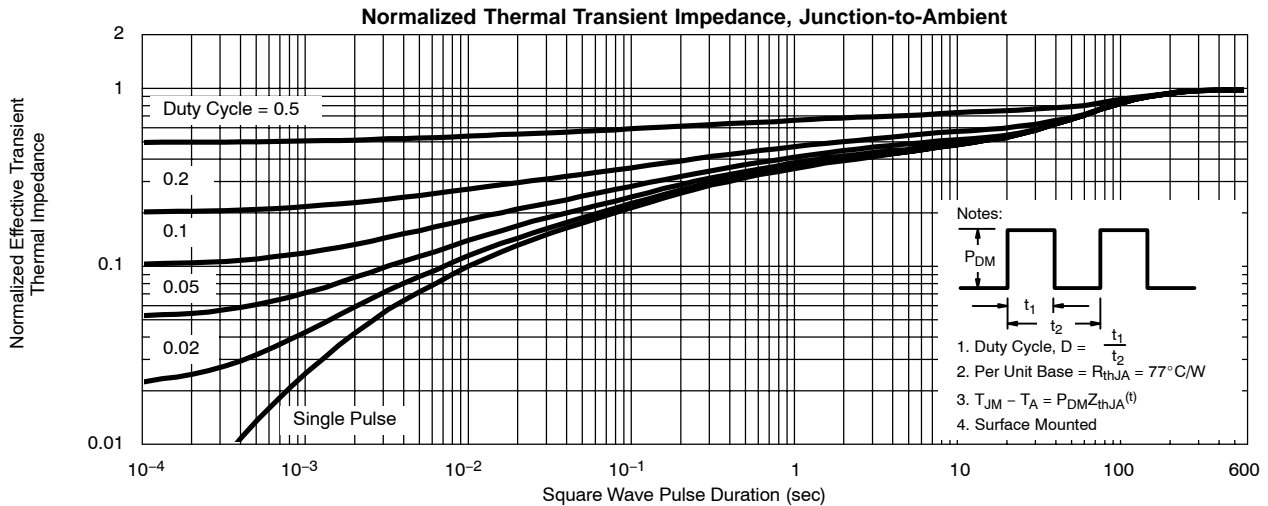
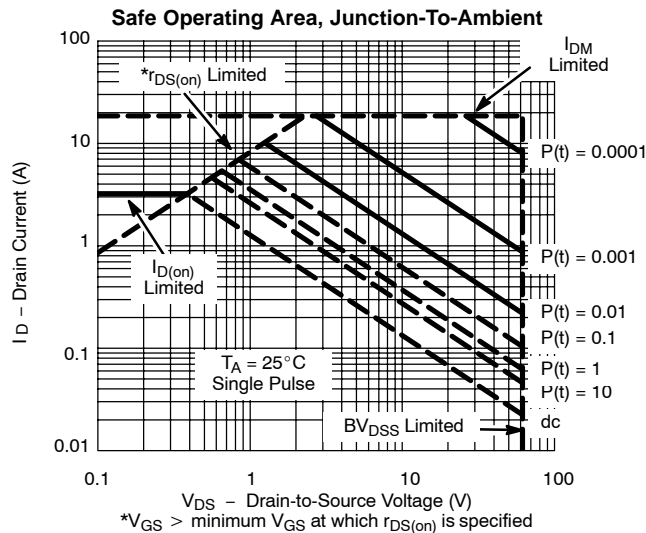
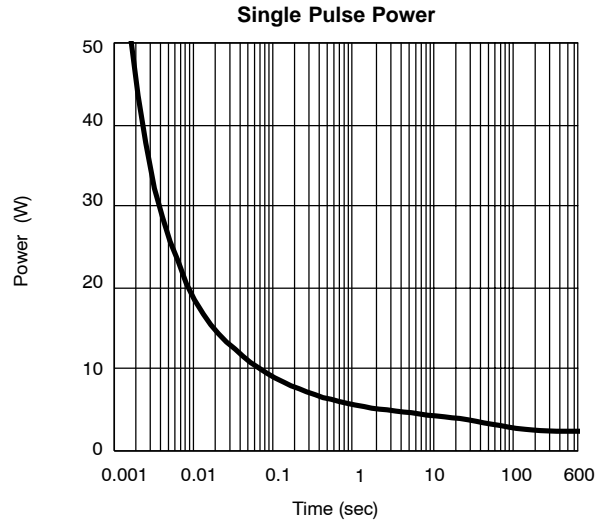
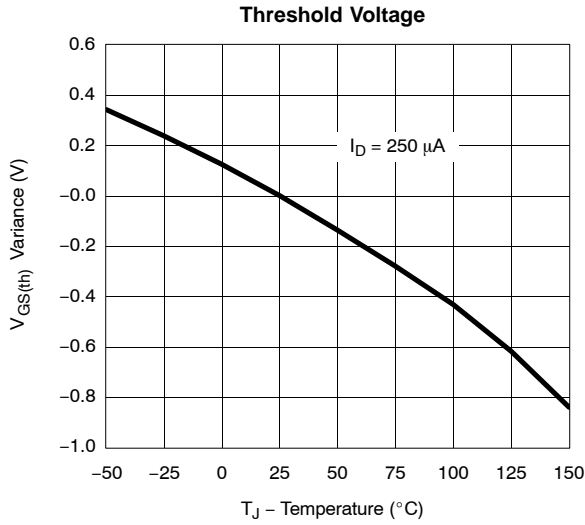




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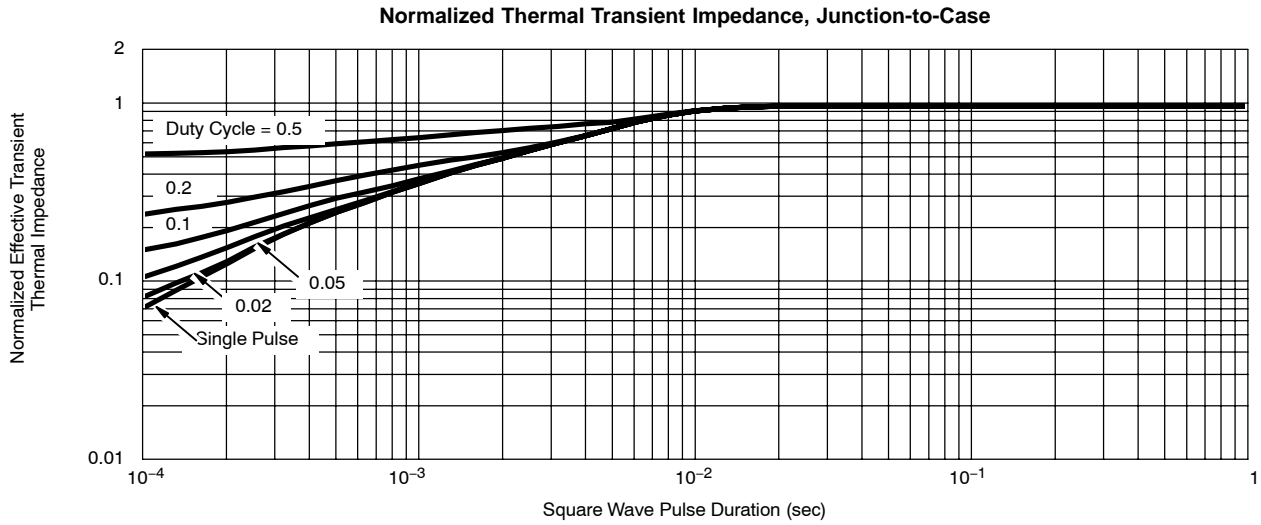
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TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



NOTE:

The minimum creepage between D1 and D2 for this 100-V device is 0.2 mm. Please see PowerPAK 1212-8 outline drawing, document # 71656, for more information.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73117>.